PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	Docket No: Q79526
Taro FUJII, et al.	
Appln. No.: 10/761,365	Group Art Unit: 2183
Confirmation No.: 3414	Examiner: Cody, Dillon J.
Filed: January 22, 2004	

For: ARRAY-TYPE PROCESSOR

AMENDMENT UNDER 37 C.F.R. § 1.111

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated April 18, 2006, please amend the above-identified application as follows on the accompanying pages.

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AMENDMENTS TO THE SPECIFICATION

Please replace the present title with the following amended title:

ARRAY-TYPE PROCESSOR IN WHICH MULTIPLE OPERATING STATES OF PROCESSOR ELEMENTS ARE SET

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): An array-type processor ~~in which~~comprising:

a multiplicity of processor elements, which individually execute data processing in accordance with instruction codes in which data are individually set, ~~are~~ said multiplicity of processor elements arranged in rows and columns~~, and~~; and

a state control unit which changes a configuration of the multiplicity of processor elements and causes successive transitions of operating states of the multiplicity of processor elements for each operating cycle by ~~means of~~ contexts that are composed of said instruction codes; wherein:

said multiplicity of processor elements are divided into a plurality of element areas;

~~one~~ said state control unit is connected to the plurality of element areas;

a prescribed number of said operating states that occur in different said operating cycles are set to at least a portion of said contexts; and

said state control unit temporarily halts operations of said element areas that correspond to a prescribed number of said operating states that are set to one said context during said operating cycles in which said operating states do not occur.

2. (currently amended): An array-type processor ~~in which~~comprising:

a multiplicity of processor elements, which individually execute data processing in accordance with instruction codes in which data are individually set, ~~are~~ said multiplicity of processor elements arranged in rows and columns~~, and~~; and

state control units which change a configuration of the multiplicity of processor elements and cause successive transitions of operating states of the multiplicity of processor elements for each operating cycle by ~~means of~~ contexts that are composed of said instruction codes; wherein:

said multiplicity of processor elements are divided into a plurality of element areas;

each of the plurality of element areas is connected to a respective state control unit of an equal number of the element areas;

a prescribed number of said operating states that occur in different said operating cycles are set to at least a portion of said contexts; and

said state control units temporarily halt operations of said element areas to which said state control units are connected, the operations of the element areas corresponding to a prescribed number of said operating states that are set to one said context, during said operating cycles in which said operating states do not occur.

3. (currently amended): An array-type processor ~~in which~~ comprising:

a multiplicity of processor elements, which individually execute data processing in accordance with instruction codes in which data are individually set, ~~are~~ said multiplicity of processor elements arranged in rows and columns~~, and~~; and

state control units which change a configuration of the multiplicity of processor elements and cause successive transitions of operating states of the multiplicity of processor elements for each operating cycle by ~~means of~~ contexts that are composed of said instruction codes; wherein:

said multiplicity of processor elements are divided into a number (a×b) of element areas;

each of a number (a) of said state control units is connected to a respective group of (b) element areas of these (a×b) element areas;

a prescribed number of said operating states that occur in different said operating cycles are set to at least a portion of said contexts;

said state control units temporarily halt operations of said element areas to which said state control units are connected, the operations of the element areas corresponding to a prescribed number of said operating states that are set to one said context, during said operating cycles in which said operating states do not occur.

4. (original): An array-type processor according to claim 1, wherein said state control units cause an operation of a portion of a plurality of processor elements of said element areas that said state control units have temporarily halted.

5. (original): An array-type processor according to claim 2, wherein said state control units cause an operation of a portion of a plurality of processor elements of said element areas that said state control units have temporarily halted.

6. (original): An array-type processor according to claim 3, wherein said state control units cause an operation of a portion of a plurality of processor elements of said element areas that said state control units have temporarily halted.

7. (original): An array-type processor according to claim 1, wherein:

a shared resource is provided that is shared by said plurality of element areas; and

said state control units switch paths to said shared resource from said plurality of element areas.

8. (original): An array-type processor according to claim 2, wherein:

a shared resource is provided that is shared by said plurality of element areas; and

said state control units switch paths to said shared resource from said plurality of element areas.

9. (original): An array-type processor according to claim 3, wherein:

a shared resource is provided that is shared by said plurality of element areas; and

said state control units switch paths to said shared resource from said plurality of element areas.

10. (original): An array-type processor according to claim 4, wherein:

a shared resource is provided that is shared by said plurality of element areas; and

said state control units switch paths to said shared resource from said plurality of element areas.

11. (original): An array-type processor according to claim 5, wherein:

a shared resource is provided that is shared by said plurality of element areas; and

said state control units switch paths to said shared resource from said plurality of element areas.

12. (original): An array-type processor according to claim 6, wherein:

a shared resource is provided that is shared by said plurality of element areas; and

said state control units switch paths to said shared resource from said plurality of element areas.

REMARKS

Claims 1-12 are all the claims pending in the application.

Initially, Applicant thanks the Examiner for acknowledging the claim to foreign priority and receipt of the priority document. Applicant additionally thanks the Examiner for initialing and returning the Forms SB/08 submitted with the Information Disclosure Statements of January 22, 2004 and October 15, 2004.

The outstanding objections and rejections are traversed, as discussed below.

Objection to the Specification

The Examiner objects to the title as being non-descriptive. Applicant has amended the title accordingly and, thus, reconsideration and withdrawal of the objection is requested.

Objection to the Claims

Applicant has revised the claim language and requests the objection be withdrawn.

Claim Rejections - 35 U.S.C. § 102

Claims 1-12 stand rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Dahl et al. (U.S. Patent No. 5,710,938, hereinafter "Dahl"). Applicant respectfully traverses and submits that Dahl fails to teach or suggest all the features of these claims, as evidenced by the following.

With respect to claim 1, a novel array-type processor is defined which presents new features. For instance, claim 1 defines an array-type processor comprising, *inter alia*, a multiplicity of processor elements, which individually execute data processing in accordance with instruction codes in which data are individually set, the multiplicity of processor elements arranged in rows and columns; and a state control unit which changes a configuration of the multiplicity of processor elements and causes successive transitions of operating states of the multiplicity of processor elements for each operating cycle by contexts that are composed of the instruction codes. Further, claim 1 recites the multiplicity of processor elements are divided into a plurality of element areas, each of the plurality of element areas is connected to a respective state control unit of an equal number of the element areas, and a prescribed number of the operating states that occur in different said operating cycles are set to at least a portion of the contexts. Claim 1 additionally recites the feature of the state control units temporarily halt operations of the element areas to which the state control units are connected, the operations of the element areas corresponding to a prescribed number of the operating states that are set to one said context, during the operating cycles in which the operating states do not occur.

Conversely, Dahl simply teaches that a data processing array is partitioned by electronic control signal into multiple sub-arrays which are established and operate independently of each other. *See* Dahl at col. 1, lines 6-11. For instance, as shown in FIG. 2a, Dahl teaches that an array 11 is partitioned into nine sub-arrays which operate independently. *See* Dahl at col. 4, lines 23-34. As taught by Dahl, by virtue of the partitioning and independent operation, data

processing nodes within each sub-array run respective programs without interfering with programs on any other sub-array. *See* Dahl at col. 4, lines 35-42.

By contrast, in the array-type processor as defined by claim 1, the contexts indicate operating states and a configuration of processor elements of the processor. Consequently, a data path may realize a plurality of states, such that a data path with inactive states may be prevented from operating in order to permit states to become active in turn. Thus, it is not necessary that a data processing array be partitioned into multiple sub-arrays which are established and operate independently, as in the data processing array taught by Dahl, which does not suggest a state control unit using contexts as claimed. Moreover, in the array-type processor of claim 1, it is not necessary that sub-arrays operate independently and operations of unnecessary parts may be halted.

Thus, Applicant submits that Dahl fails to teach or suggest at least the feature of a state control unit which changes a configuration of the multiplicity of processor elements and causes successive transitions of operating states of the multiplicity of processor elements for each operating cycle by contexts that are composed of said instruction codes, as claimed. As a consequence, Dahl further fails to teach the features of a prescribed number of said operating states that occur in different said operating cycles are set to at least a portion of said contexts; and the state control unit temporarily halts operations of the element areas that correspond to a prescribed number of the operating states that are set to one said context during the operating cycles in which the operating states do not occur.

In view of the foregoing, reconsideration and withdrawal of the rejection of claim 1 is requested. With respect to independent claims 2 and 3, Applicant submits that these claims likewise recite features that are neither taught nor suggested by Dahl for reasons analogous to those discussed above.

With respect to dependent claims 4-12, Applicant submits that these claims are allowable at least by virtue of their dependency and by virtue of the features recited therein.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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WASHINGTON OFFICE
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CUSTOMER NUMBER

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